

Remarks

Applicants respectfully request reconsideration of this application as amended. Claims 5, 10 and 22 have been amended. No claims have been cancelled. Therefore, claims 1-26 are presented for examination.

Claims 1-6, 10-13, 18-21 stand rejected under 35 U.S.C. §102(b) as being anticipated by Wells et al. (U.S. Patent No. 5,535,369). Applicants submit that the present claims are patentable over Wells.

Wells discloses the performance enhancement of a solid-state disk by storing repeatedly used information in a RAM. The information is referred to as FLASH array database. Further, Wells discloses that a sector header translation table (SHTT) also stored in RAM that translates a sector number into a pointer to an associated sector of data. Both the FLASH array database and SHTT must be generated during power-up because they are stored in volatile memory, RAM, and because reads and writes depend upon them. First, building begins with the initialization of the SHTT. Each pointer for each sector number is set to the same initial value. Next, the total amount of free memory within the FLASH array, and the total amount of free memory per chip are initialized to their maximum values. See Wells at col. 7, ll. 20 – col. 8, ll. 55.

Claim 1 recites halting the downloading of data into a flash memory until the flash memory is initialized, wherein the initialization includes storing pointers in a memory to different locations within the flash memory where the data is to be stored. Applicants submit that Wells does not disclose such a limitation. Wells discloses a FLASH array database and sector header translation table stored in memory. Nonetheless, there is no disclosure of halting the downloading of data into a flash memory until the flash memory is initialized. Therefore, claim 1 is patentable over Wells.

Claims 2-4 depend from claim 1 and include additional limitations. Thus, claims 2-4 are also patentable over Wells.

Claim 5 recites, initializing a flash memory of a device prior to receiving data in response to receiving a request to store data at the flash memory. Applicants submit that Wells does not disclose its initialization process in response to receiving a request to store data at the flash memory. As a result, claim 5 is patentable over Wells. Because claims 6-9 depend from claim 5 and include additional limitations, claims 6-9 are also patentable over Wells.

Claim 10 recites an initialize unit to initialize a flash memory in response to receiving a request to download data. Thus, for the reasons described above with respect to claim 5, claim 10 is patentable over Wells. Since claims 11-13 depend from claim 10 and include additional limitations, claims 11-13 are also patentable over Wells.

Claim 14 recites a processor to halt the downloading of data into a flash memory until the flash memory is initialized, wherein the initialization includes storing pointers in the random access memory to a number of the blocks within the flash memory where the data is to be stored. For the reasons described above with respect to claim 1, claim 14 is patentable over Wells. Because claims 15-17 depend from claim 14 and include additional limitations, claims 15-17 are also patentable over Wells.

Claim 18 recites halting the downloading of data into a flash memory until the flash memory is initialized, wherein the initialization includes storing pointers in a memory to different locations within the flash memory where the data is to be stored. For the reasons described above with respect to claim 1, claim 18 is patentable over Wells. Because claims 19-21 depend from claim 18 and include additional limitations, claims 19-21 are also patentable over Wells.

Claim 22 recites initializing a flash memory of a device prior to receiving data in response to receiving a request to store data at the flash memory. Thus, for the reasons described above with respect to claim 5, claim 22 is patentable over Wells. Since claims 23-26 depend from claim 10 and include additional limitations, claims 23-26 are also patentable over Wells.

Claims 7-9, 14-17, 22-26 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Wells et al. (U.S. Patent No. 5,535, 369) in view of See et al. (U.S. Patent No. 6,189,070). Applicants submit that the present claims are patentable over Wells even in view of See.

See discloses a method and apparatus that manages data and reads code from a nonvolatile writeable memory. See See at Abstract. Nevertheless, See does not disclose or suggest halting the downloading of data into a flash memory until the flash memory is initialized, wherein the initialization includes storing pointers in a memory to different locations within the flash memory where the data is to be stored. Moreover, See does not disclose or suggest initializing a flash memory of a device prior to receiving data in response to receiving a request to store data at the flash memory.

As discussed above, Wells also does not disclose or suggest such limitations. Therefore, any combination of Wells and See would also not disclose or suggest halting the downloading of data into a flash memory until the flash memory is initialized, wherein the initialization includes storing pointers in a memory to different locations within the flash memory where the data is to be stored, or initializing a flash memory of a device prior to receiving data in response to receiving a request to store data at the flash memory. Consequently, the present claims are patentable over Wells in view of See.

Applicants respectfully submit that the rejections have been overcome, and that the claims are in condition for allowance. Accordingly, applicants respectfully request the rejections be withdrawn and the claims as amended be allowed.

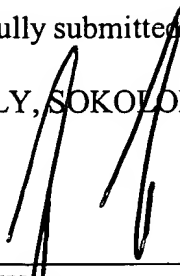
The Examiner is requested to call the undersigned at (303) 740-1980 if there remains any issue with allowance of the case.

Please charge any shortage to our Deposit Account No. 02-2666.

Respectfully submitted,

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